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Digital Synchronization System Design and Implementation for Radio Interferometer

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Abstract

Recent advances in technology research have low cost, low power in radio interferometer network. Clock synchronization is an important service in any distributed system, including radio interferometer systems. Application of clock synchronization includes high frequency up to 1 GHz digital synchronous data transmission from antennas to central Master. However, most distributed synchronization algorithms cannot satisfy the requirement for high speed interferometer network system, such as PTP (Precision Time Protocol). This work describes new concept clock synchronization for future wideband radio interferometer and sensors network with consideration about the requirements. Finally, we propose hardware architecture prototype for clock synchronization, based on TDC (Time-to-Digital Converter), DTC (Digital-to-Time Converter) and FPGA (Field-Programmable Gate Array) circuits. Simulation results are given to corroborate the proposed algorithm and analysis.

1 Introduction

The Nançay Radio-heliograph [1] is a radio telescope consisting of 48 distributed in two perpendicular branches forming a 'T': 19 branches in East-West spread over 3200 m, and 25 parabolic antennas divided into North-South on 2440 m. Radio Frequency (RF) signals provided by coaxial cable from antennas to a central Master. The hardware correlation of the recorded signals allows building 11 radio images from 150 to 450 MHz with 1 MHz fixed frequency resolution to observe solar corona and eruptions [2]-[3].

Recently, the demand for high accuracy common time reference within distributed networks has intensified; also it is important issue in communication networks. Furthermore, clocks with high accuracy offset measurement and calibration will play a major role in synchronous networks. These solutions require more accurate and stable centralized clocks with offsets down to $10^{-10}s$ [4]. Currently, high accuracy timestamps measurement and clock synchronization used in a vast diversity of applications. Examples of these include clock synchronization in White Rabbit (WR) multi-company and multi-laboratory project [5]. The main advantage of this protocol is their ability to achieve sub-ns accuracy and Pico-second jitter based on time transfer over Ethernet, such as IEEE 1588 (Precision Time Protocol) and synchronous Ethernet [6]-[8]. The purpose of this research is to explore a new technical concept for future radio astronomy instruments with dynamic frequency resolution. The mechanism is applied to solar interferometer and examines new digital system requirements.

The main contributions of this paper are twofold. First, we propose new synchronization mechanism and hardware architecture for 1 GHz A/D converter sampling frequency used for each antenna. It cannot only improve clocks offset estimation basing on timestamps measurement with 13 ps accuracy, but also reduce the computational complexity with FPGA implementation. Second, simulation, time measurement board, offset computation and compensation strategy are conducted to demonstrate the efficacy of the proposed scheme. In this work, clocks synchronization algorithm focused on the central Master. Also, all clocks are derived from a stable and accurate source based on Rubidium controlled by GPS (Global Positioning System) [9].

2 Clock synchronization system accuracy requirement

In this section we compute system accuracy requirement basing on interferometry principle [10]. Let's consider two parabolic antennas A_n and A_{n+1} , spaced by $D(m)$. The plane wave coming from the source in the sky, reached A_n antenna after τ_g delay, then:

$$\begin{cases} D_c = D.cos(\theta) \\ D_s = D.sin(\theta) = c.\tau_g \end{cases} \quad (1)$$

Given two signals $x_n(t)$ and $x_{n+1}(t)$ with :

$$\begin{cases} x_n(t) = E_n.cos(2\pi ft) \\ x_{n+1}(t) = E_{n+1}.cos(2\pi f(t-\tau_g)) \end{cases} \quad (2)$$

Considering τ_n and τ_{n+1}, two errors induced by offset compensation between A_n and A_{n+1} antennas. We assume the differential error $\delta\tau_g = \tau_n - \tau_{n+1}$ and $t_0 = t - t_1$, while, the output of correlator $r(\tau_g)$ is given by the following formula (10) :

$$r(\tau_g) \infty \frac{E_n E_{n+1}}{2} [cos(2\pi f \tau g (1 - \frac{\delta \tau g}{\tau g}))] \quad (3)$$

Differential error $\delta\tau_g$ for 5% equal to 112 picoseconds, it is 50 at 1% of the loss correlation rate $r(\tau_g)$ using 450 MHz maximal analog frequency.

3 Synchronization algorithm

The Master are the core of the system Fig. 1, measure round trip delay for each antenna with picoseconds accuracy using TDC board. In this work we used quad channel time measurement TDC. This device includes four timestamps measurement channels (Events) with synchronization channel (Sync) optimized to make picosecond accuracy time-interval measurements based on hardware interpolation method. The TDC board includes a high-speed serial interface to a host processor (up to 50 Mb/s). There is one central controller which then drives registers, counters, etc., in each channel. The configuration interface is used for writing or reading registers that reside in the TDC chip. These allow configuration of the device functions. Register addresses are 8 bits long. Data words are 16 bits wide, enabling more-efficient interface transactions.

Considering the round trip delay T_i for each antenna $(i, 1...n)$. Present delay from master to master (d_{MM}). d_{MM} measured by TDC is given by the following formula :

$$d_{MM} = d_{MS} + d_{SM} \quad (4)$$

- d_{MM} Master to Master delay
- d_{MS} Master to Slave delay
- d_{SM} Slave to Master delay

Eqs. (4) present basic model delay. d_{MS} include transmission delay from TDC to channel and reception delay from channel to slave, same for d_{SM}.In any case $d_{MS} \neq d_{SM}$ this presents a problem for antennas synchronization. The Following section will be dedicated to explain how to calculate the average difference δ_0^i between d_{MS} and d_{SM}, also how to calibrate offsets between master and slaves (antennas). Assumed that $d_{SM}^i > d_{MS}^i$ and :

$$\begin{cases} d_{MS}^i = \delta_i \\ d_{SM}^i = \delta_i + \delta_0^i \\ d_{MM} = 2\delta_i + \delta_0^i \\ T_i = d_{MM} \end{cases} \quad (5)$$

Where δ_0^i defined offset delay between master and slave $(\delta_0^i = d_{SM}^i - d_{MS}^i)$.

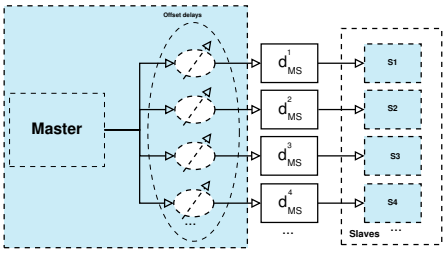

Figure 1. Offset delays injection architecture for global synchronization.

3.1 Synchronization condition

The synchronization algorithm compute offsets for each antennas (Fig. 1) to achieve global synchronization. The synchronization procedure is as fallows :

Where T_i' defined delay between master and antenna (i) after synchronization phase.The difference between each delay pair T_i' and T_{i+1}' is given by :

$$\Delta T_{i,i+1}' = T_i' - T_{i+1}' = \frac{1}{2}[T_i - T_{i+1}] = \Delta T_{i,i+1} \quad (6)$$

For global synchronization, it is necessary to set to zero time difference between each antenna pair, the condition is given by the following formula :

$$\Delta T_{i,i+1}' = 0 \quad (7)$$

Eqs. (8)-(12) shows how to synchronize between two antennas.

$$\Delta T_{1,2}' = T_1' - T_2' \Rightarrow T_1 = T_2 \quad (8)$$

$$\Rightarrow 2\delta_1 + \delta_0^1 = 2\delta_2 + \delta_0^2 \Rightarrow \delta_1 + \frac{1}{2}\delta_0^1 = \delta_2 + \frac{1}{2}\delta_0^2 \quad (9)$$

Let's insert two unknown delays δx_1 and δx_2, because the delay path cannot be assumed symmetric for varying cable length and times delays between master and slaves, then:

$$\delta_1 + \frac{1}{2}[\delta_0^1 + \delta x_1] = \delta_2 + \frac{1}{2}[\delta_0^2 + \delta x_2] \quad (10)$$

$$\Rightarrow \delta x_1 = T_2 - T_1 + \delta x_2 \Rightarrow \delta x_1 = \Delta T_{1,2} + \delta x_2 \quad (11)$$

$$\delta x_i = \Delta T_{i,i+1} + \delta x_{i+1} \quad (12)$$

Calibration vector for N antennas Eqs. (14)-(15) :

$$\begin{cases} \delta x_1 = \Delta T_{1,2} + \delta x_2 \\ \delta x_2 = \Delta T_{2,3} + \delta x_3 \\ \dots \\ \delta x_{N-1} = \Delta T_{N-1,N} + \delta x_N \end{cases} \quad (13)$$

$$\begin{bmatrix} \delta x_1 \\ \delta x_2 \\ \dots \\ \delta x_{N-1} \end{bmatrix} = \begin{bmatrix} \Delta T_{1,2} \\ \Delta T_{2,3} \\ \dots \\ \Delta T_{N-1,N} \end{bmatrix} + \begin{bmatrix} \delta x_2 \\ \delta x_3 \\ \dots \\ \delta x_N \end{bmatrix} \quad (14)$$

3.2 Offsets computation

After measurement of all delays T_i for each antenna. The delay vector is sorted in ascending order. The last value of the vector is defined as being the reference calculation (initialization value) for δx_i with maximum delay, in this case, $\delta x_N = 0$. Taking an example with four antennas, with the values measured by the TDC with $LSB = 13ps$ accuracy for each antenna pair T_i $(i = 4..1)$:

- Initial conditions : $T_i = (15, 10, 8, 5)$
- δx_i computation : $\delta x_i = (0, 5, 7, 10)$
- T_i calibration : $A_i : T_i' = T_i + \delta x_i = 15$

After offsets adjustment, all clocks arrived at the same time at each antennas Fig. 2.

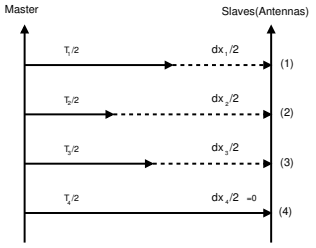

Figure 2. Timing diagram clocks offset adjustment.

3.3 Simulations and results

Eqs. (12) can be written as follows :

$$\delta x_i = \delta x_{i-1} - \Delta T_{i,i-1} \quad (15)$$

The Z-transform of Eqs. (15) :

$$\delta X(Z) = Z^{-1}\delta X(Z) - (T(Z) - Z^{-1}T(Z)) \quad (16)$$

Fig. 3 present bloc diagram for Eqs. 25, with :

- $T = [T_1, T_2, ...T_N]$
- $d_x = [\delta x_1, \delta x_2, ...\delta x_N]$

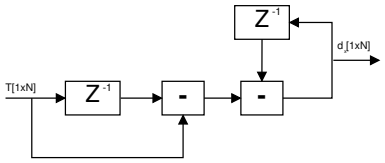

Figure 3. Offsets computation algorithm bloc diagram.

Input delays T_i format from TDC and output offsets δx_i (Fig.4) :

$$T\_in = \begin{bmatrix} T_1 \\ T_2 \\ \dots \\ T_N \end{bmatrix}, d\_out = \begin{bmatrix} \delta x_1 \\ \delta x_2 \\ \dots \\ \delta T_N \end{bmatrix}$$

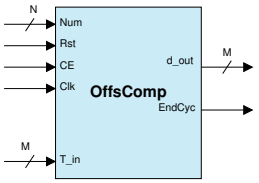

Figure 4. Offsets computation entity.

The Fig. 4 shows synchronous offsets computation device and their implementation in FPGA Virtex-6. M presents timestamps measurement length (T_in) and offsets computation output (d_out). $EndCyc$ indicate end of offsets calculation. For each clock event, $OffsComp$ receive multiplexed and synchronous timestamps (T_i) and generate offset equivalent output (δ_i)

Simulation results for N=3 bits and M=40 bits using. The algorithm is implantable in FPGA. The maximum frequency of the architecture equal to 270.63 MHz for N=3, M=40 and 455.78 MHz for N=3 and M=4. The frequency decreases with increasing size of the data bus, it goes from 455 MHz for M=4 bits to 240 MHz for M = 64 bits. It remains constant when the number of slaves (N) changes Fig.5.The number of Flip-Flops registers increase with M, it goes from 20 (M=4, N=3) to 260 (M=64, N=3).It also increases slowly with N.

Slice Logic Utilization	Used	Utilization
Number of Slice Registers	494	1%
Number of Slice LUTs	507	1%
Number of LUT Flip Flop pairs used	595	1%

Table 1. Slice Logic Utilization

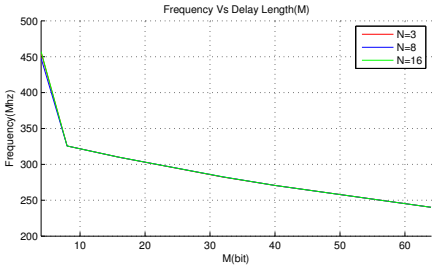

Figure 5. Frequency (MHz) Vs delay length M in bit for N=[3, 8 or 16 bits].

3.4 Master hardware architecture description

The Fig. 6 shows the master global synchronization architecture circuit. The individual synchronization of each antenna is achieved by integrating delay calculated by the previous algorithm in DTC circuit. For global synchronization, we integrate all delays in DTC and start all channels with a single signal (Sync) Fig. 6 coming from FPGA device. DTC circuitry used in this work have 10 ps accuracy with 10 bits resolution, controlled by a highly accurate synchronizing signal derived from the rubidium source clock. The distribution of accurate clocks has achieved by Fanout Buffers.

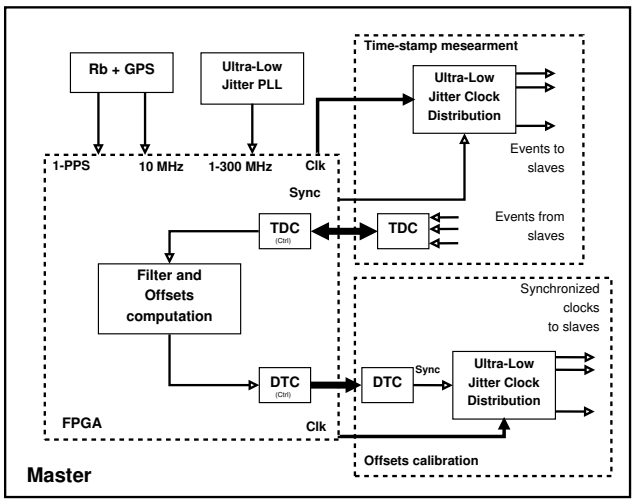

Figure 6. Time-stamp measurements and clocks offset calibration architecture.

4 Conclusion

In this paper, we present and analyse digital architecture for future radio interferometer feasibility in 150-450 MHz frequency band. The synchronization circuit requires 50 ps accuracy accepting 1% loss correlation ratio. We contribute in this work to the development of a new synchronization algorithm for distributed clocks and their simulation and implementation in Virtex 6 FPGA. The offsets computation unit supports 270 MHz with 40 result bits, the number of antennas has no effect in frequency. We have described also a global system architecture for clock synchronization with 10 ps accuracy. The hardware architecture is based on subnanosecond TDC, DTC circuits. The hardware test board development for master architecture is ongoing. We are currently working in delay compensation and global architecture offsets calibration from TDC circuit. We would like to estimate errors with Gaussian distribution, then, compensate following data to get more accuracy for global clocks synchronization.

Acknowledgments

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