A Low Phase Noise Low Power Fractional-N Synthesizer Architecture

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The new Fractional-N synthesizer architecture will be presented. The synthesizer achieves low fractional spurs and quantization noise, which relaxes the trade-off between phase locked loop bandwidth and phase noise. Proposed architecture is based on two delay lines, which are used to compensate phase error resulting from fractional synthesis.

Fractional-N synthesizers are widely used in wireless communication integrated transceivers. Typically they are used as local oscillator. In the case when frequency or phase modulation is used in communication system, the Fractional-N synthesizers are used as modulators. In such a case new trade-off emerges between phase noise and synthesizer bandwidth.

The proposed architecture substantially reduces phase noise of the Fractional-N synthesizer thus relaxing the trade-off between phase noise and synthesizer bandwidth. The proposed synthesizer architecture is presented in Fig. 1. New parts that were added to the standard Fractional-N synthesizer are indicated by the shaded blocks. These blocks are: two delay lines with K unit delay elements, control block and calibration block. Delay lines are used to generate linearly increasing phase error at the phase detector (PFD & CP) input. According to the PLL dynamics this phase error will produce frequency shift at the synthesizer output. This shift will be proportional to increase rate of the phase error. For proper delay values, $1/K/F_{out}$ and $(K+1)/K^2/F_{out}$, the frequency tuning step of the synthesizer is equal to F_{ref}/K^2 and no additional phase noise is produced. The calibration block is employed to ensure that the unit delay in each delay line has proper value.

Unfortunately due to limited calibration accuracy and components mismatch, unit delays differ from their nominal values. Moreover, delay lines introduce additional jitter at the input of the phase detector. To analyze impact of these nonidealities a noise model was developed and analyzed. The results of this analysis are promising and will be presented during the conference.

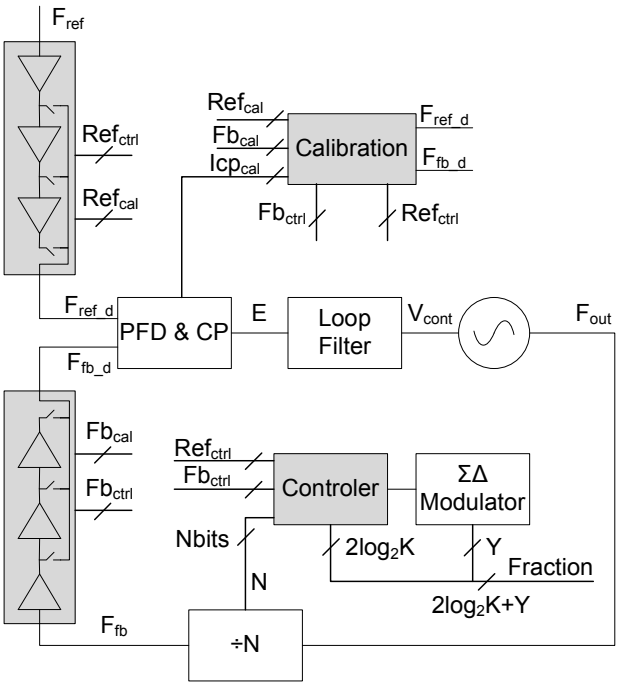

Fig. 1. The proposed Fractional-N synthesizer architecture