Design and performance measurements of an FPGA accelerator for a 100Gbps wireless data link layer

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To achieve 100Gbps wireless transmission, not only a very fast physical layer is required. The effort of the analog transceiver can be wasted due to the overhead induced by the higher network layers. Delays and latencies caused by a duplex switching can dramatically reduce the goodput of the link. In every microsecond of a delay, 12.5kB of the data transfer is wasted. Therefore, we need to extend the frame size, but that will lead to a higher packet error rate.

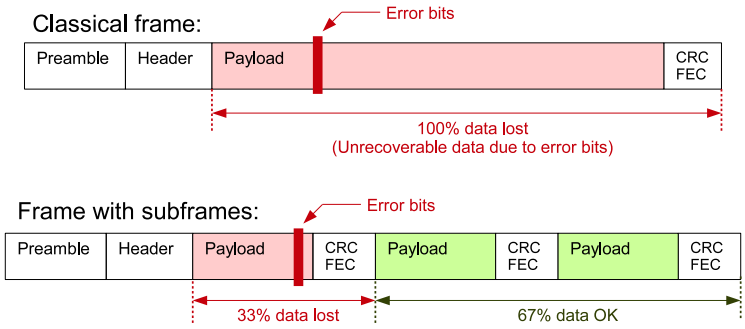

Figure 1. An explanation how the subframes can improve the total efficiency. In a case of bit errors in a classical frame, the whole payload has to be retransmitted. If the subframes are used, then only the invalid part is rejected and there is no need to retransmit the whole frame, only the defect part.

To achieve the highest user data throughput, we reduced the overhead induced by the protocol. It means that the payload dominates in the frame and the frame size is increased. We share a single preamble and protocol header for multiple frames. The percentage of user data per packet is increased. This approach has advantages on links with a relatively low bit error rate. If the channel quality is low (high bit error rate), then this solution will reduce the goodput or will block the link completely. This situation can be explained by statistical analysis. If the payload is larger, the probability that at least one bit will be altered due to channel conditions is higher. The recalculated checksum is invalid and the whole frame has to be discarded. To deal with this problem, we have employed two additional techniques. Firstly, we use a frame with subframes. The frame is divided into subframes and the subframes can be selectively repeated. This allows to retransmit only a small part of the defect frame (please see Fig. 1). Additionally, we can change the subframe size to improve the communication robustness. The second technique is forward error correction. We add some redundant data to the subframes. After that, the receiver can use this additional information to locate the bit errors and fix them. The forward error correction in our implementation can fix only a few symbols. The correction capabilities are restricted by the redundant information size and calculation power. To reduce the negative impact of these factors, we can adopt the error correction effort to the channel quality.

In our paper we present results of implementation and validation of the data link layer accelerator for 100 Gbps wireless transmissions. The accelerator can be used to speed up a forward error correction for the hybrid automatic repeat request and is fully implemented in VHDL. We have achieved 38.6 Gbps with Reed-Solomon coding on a single Virtex7 device. The accelerator can operate at links with a bit error rate equal to or less than $2*10^{-3}$ with an efficiency higher than 80%.