



## A New Multi-Channel RF Sampling Digital Back-end for Radio Astronomy

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The recent introduction by Xilinx of its range of RF System-on-Chip (RFSoc) devices is resulting in a fundamental shift in the way digital back-ends for radio astronomy instruments are being architected. The bringing together of 8 or 16 multi-Giga-sample per second Analogue to Digital Converters (ADCs) with large and feature rich Field Programmable Gate Array (FPGA) fabric and quad-core ARM processors all on a single chip has opened up new possibilities in high-performance, power-efficient RF sampling digital systems for radio astronomy.

In this paper we present a new architecture for an RF sampling, multi-channel digital back-end for radio astronomy applications. The new system, called *Bluering*, is designed to be scaled to suit the growing trend in radio astronomy instrumentation towards large numbers of active receiving elements such as aperture arrays and phased-array feed systems.

Comprised of single-RFSoc 16-channel modules and wideband RF signals from mating RF over Fiber (RFoF) optical receiver boards, the *Bluering* system can be scaled to perform the digitization and beamforming on up to 512 RFoF signals over 300 MHz of bandwidth in a 600x600mm form factor. An overview of the *Bluering* dataflow and interfaces is provided in Figure 1. The system design builds on the inherent efficiency and analog integration of RFSoc devices using proven concepts in liquid cooled heatsinks, RFoF receivers and optical transceivers to meet the stringent power budgets and RFI emissions constraints required for radio astronomy telescopes. The performance gains and flexibility of the *Bluering* system could be used to meet the challenging low cost and low power requirements of the SKA Low Array Receiver and Beamformer [1] and provide a compact solution for future cryo-PAF systems and back-end upgrades of existing radio astronomy instruments.

We outline the potential processing capabilities of the *Bluering* architecture and present detail on the current system prototype. Design challenges regarding system cost, power, cooling, EMI and implementing custom designs with the Xilinx RFSoc will be discussed.

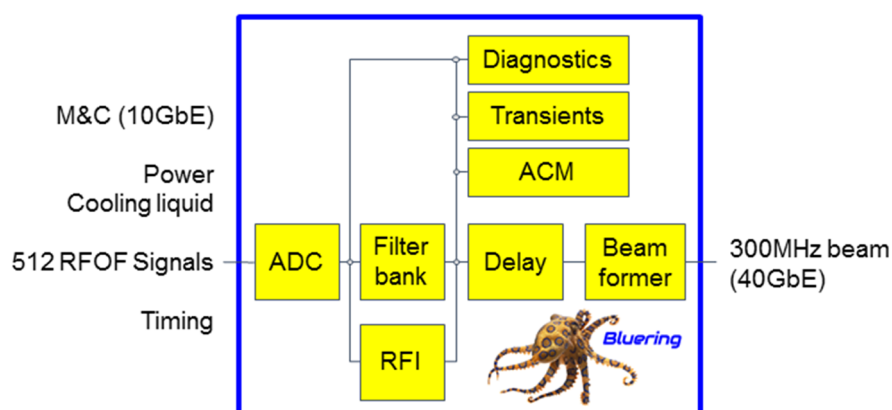


Figure 1. *Bluering* system signal processing and external interfaces

[1] G. A. Hampson, “An Integrated Low Power SKA Low Array Receiver and Beamformer,” *PAF Workshop 2018 - FAST China*, September 2018, doi: 10.13140/RG.2.2.29841.07528.